UGD-0344A

5.25 INCH FLEXIBLE DISK DRIVE

TECHNICAL MANUAL

MF504A-3

MITSUBISHI ELECTRIC CORPORATION

CONTENTS

CHAPTER 1 OUT LINE

1. This section deals with the mechanical parts and control circuits of the MF504A-3 flexible disk drive. MF504A-3 flexible disk unit with high density medium allows for more than 1MB formatted memory capacity. It is format compatible with a 8 inch flexible disk allowing the reading and writing of previously used normal density disks. However, normal density 48TPI medium can only be read. The rotational speed can be switched by an external signal for 360/300rpm for high and normal density respectively. The READ/WRITE circuitry is also automatically switched at the same time.
In addition, it is also posible to set the unit for normal density so that the rotational speed remains at 360rpm and only the READ/WRITE circuit is switched.

1.1 Composition of mechanism by Function

The mechanism can be divided by funciton as follows:

(1) Lever mechanism and door sw mechanism

(2) Disk rotation and clamp mechanism

(3) Magnetic head positioning mechanism

(4) Magnetic head/carriage mechanism

(5) Sensors (index, write protect, track 00)

1.2 Composition of Electronic Circuitry by Function

The electronic circuits are installed on two printed-circuit boards and can be classified by function as follows: The spindle motor drive circuit constitutes an independent printed-circuit board which is built integrally with the motor.

(1) Signal interface circuit and drive select circuit

(2) Power-on reset circuit

(3) Panel indicator drive circuit

(4) Index pulse generator circuit and ready circuit

(5) Step motor drive circuit

(6) Track 00 detection circuit

(7) Side select circuit

(8) Write/erase circuit

(9) Write-protect circuit

(10) Read circuit

(11) Spindle motor drive circuit

CHAPTER 2 DESCRIPTION OF MECHANISM OPERATION

Figure 2-1 shows an exploded view of the mechanism.

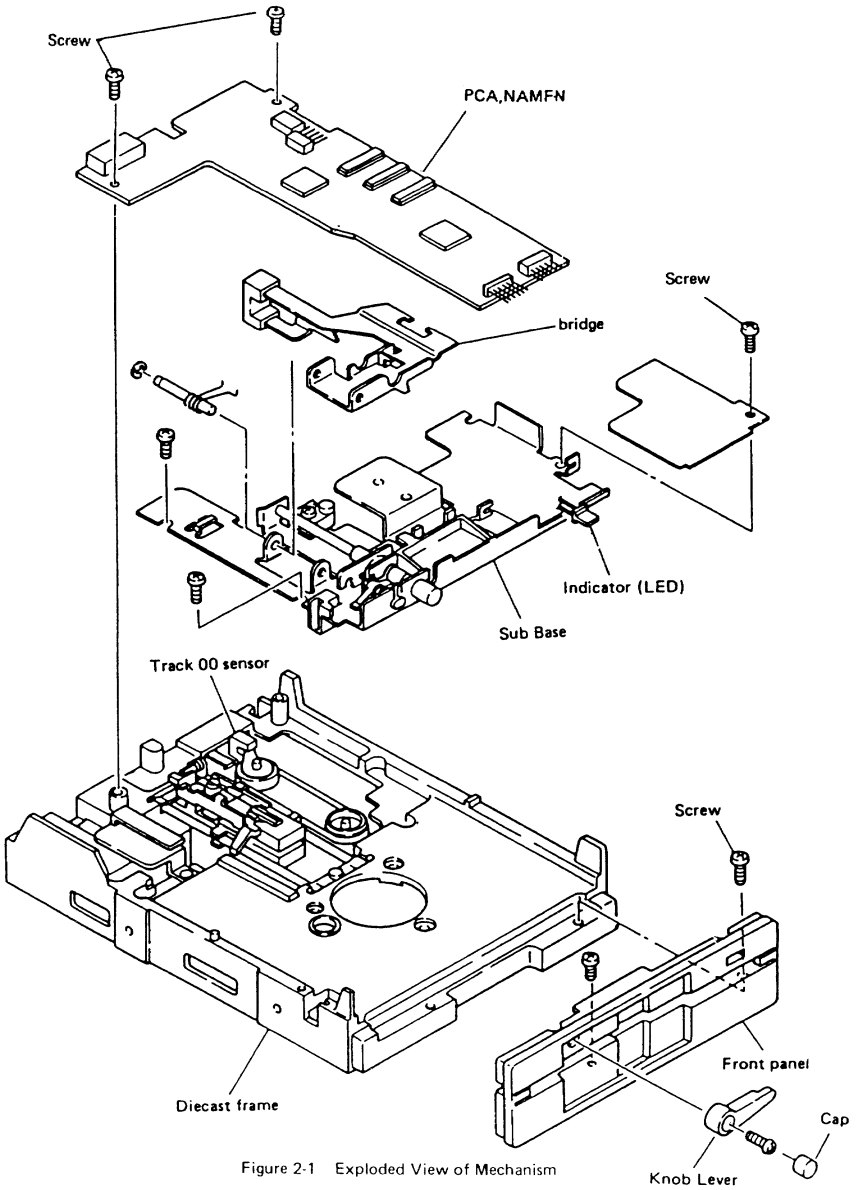


Figure 2-1 Exploded View of Mechanism

2.1 Disk Rotation Drive and Clamp Mechanism

The disk rotation drive motor is a flat DC servo motor. This motor has as long a life as an ordinary AC motor because it is a brushless type that uses a Hall element for coil phase-switching detection.
The motor does not use a belt, unlike conventional counterparts, but is a direct-drive type with the rotor and spindle directly connected to each other. This is another feature for prolonging motor life and assuring that the rotation mechanism is completely free of maintenance. The rotational speed of the spindle motor is 360rpm and 300rpm and this can be swiched by the PCA, NAMFM signals from the main control circuit.
The frequency-generator coil detects the spindle motor speed and forms a servo circuit to control it.
The disk is clamped by the spindle cone on the motor side and by the collet on the door. The collet guides the disk to a position on the inner surface of the spindle cone. This assures compatibility between diskettes and the disk drives.
The collet is tapered to a specific angle to correct non-alignment of an inserted disk with the spindle cone.
Figure 2-2 shows the spindle motor and collet.
The printed-circuit board for the spindle motor servo circuit has an index sensor LED (light-emitting diode) for disk rotation detection, write protect sensor LED for write protect defection and indicator LED for driving signal. And a photo transistor for receiving its light is installed on another printed-circuit board (NAMFM).

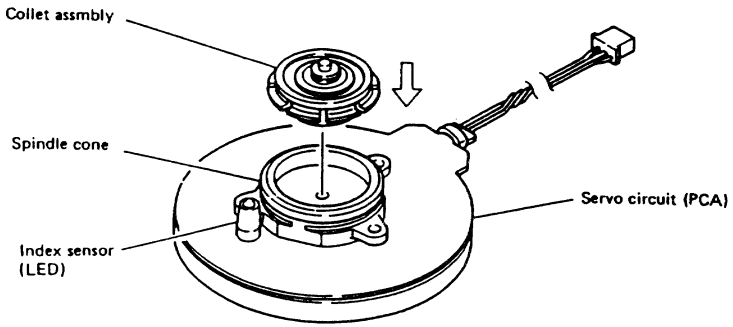


Figure 2-2 Spindle Motor and Collet

2.2 Magnetic Head-Positioning Drive Mechanism

The flat step motor drives the magnetic head to each track (cylinder) in succession. The capstan mounted on the step motor shaft has a thin-loop steel band, which is pulled by the spring attached to the idler pulley located opposite the steel band to maintain a specific tension. The head/carriage assembly, supported by two guide rods, is fastened to the steel band so that a turn of the step motor by one step angle moves the head by a single track distance.

Figure 2-3 shows the positioning drive mechanism.

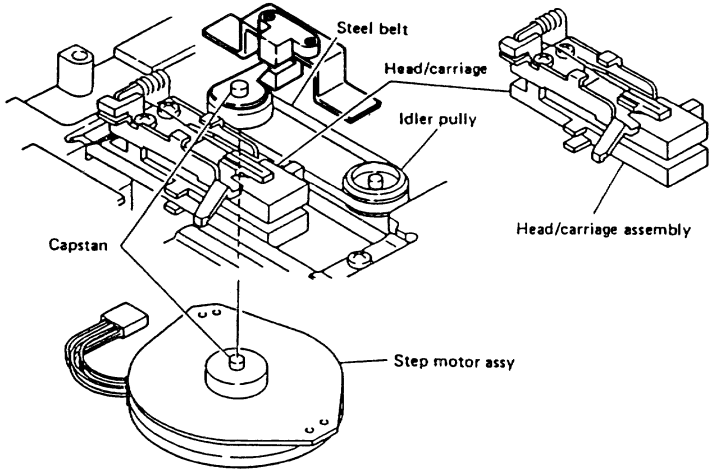


Figure 2-3 Magnetic-Head Positioning Mechanism

2.4 Sansors (Index, Write Protect, Track 00)

(1) Index sensor

The index sensor detects disk rotation. This sensor consists of an LED on the light-emitting side and a photo transistor on the light-receiving side. The LED is mounted on the servo circuit PCA for the spindle motor(Figure 2-2), and the photo transistor is mounted on the main control circuit PCA (NAMFM).

Index sensor timing (position) can be adjusted by loosening the screws on the index seonsor and removing index sensor.

Figure 2-6 shows where the photo-transistor for the index sensor is mounted.

(2) Write-protect sensor

The write-protect sensor detects the diskette's write-protect notch and inhibits write operation.

This sensor protects information stored on read-only disks from destruction by operation errors.

Disks with the diskette's notch covered with tape or a seal that does not transmit light are protected by this sensor. Remember that vinyl or cellophane tape that has a high percentage of light transmission will not protect the disk. The write-protect sensor is mounted on sub-base ash shown in Figure 2-6. [Attached to the sub-base, this will transmit signals to PCA.]

(3) Track 00 sensor

The track 00 sensor detects that the head is on track 00

The track 00 sensor detects the position of the light-shielding plate that projects from the head/carriage assembly. The sensor is screwed to the STM. holder and can be adjusted in position by loosening the screw.

The track 00 sensor and head/carriage assembly are shown in Figure 2-7.

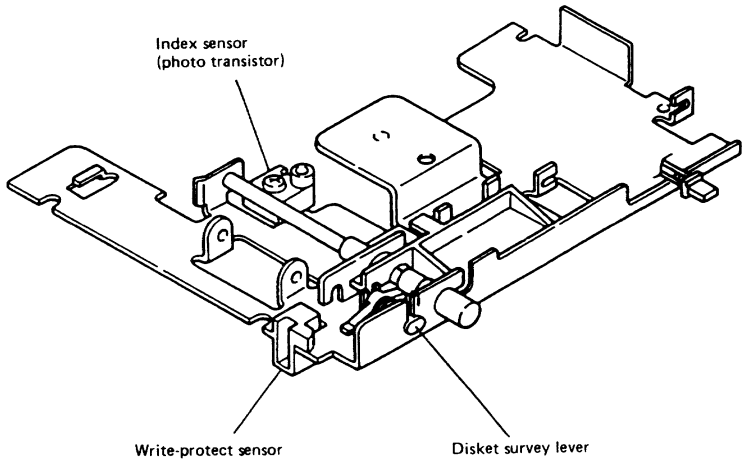


Figure 2-6 Index Sensor and Write-protect sensor

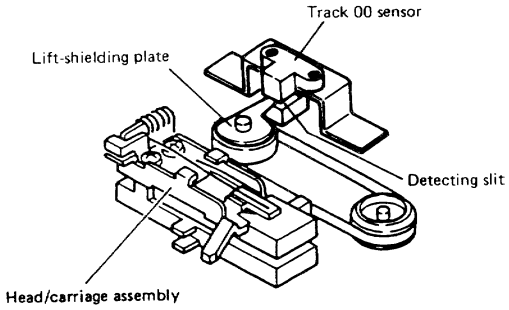


Figure 2-7 Track 00 Sensor and Head/Carriage Assembly

CHAPTER 3 DESCRIPTION OF ELECTRONIC CIRCUIT OPERATION

Figure 3-1 shows the electronic circuits and signal connections among these circuits.
The spindle motor drive circuit within the dotted lines constitutes the separate printed-circuit board that is built integrally with the motor.
The parts within the chain lines belong to the mechanism described in the previous pages.

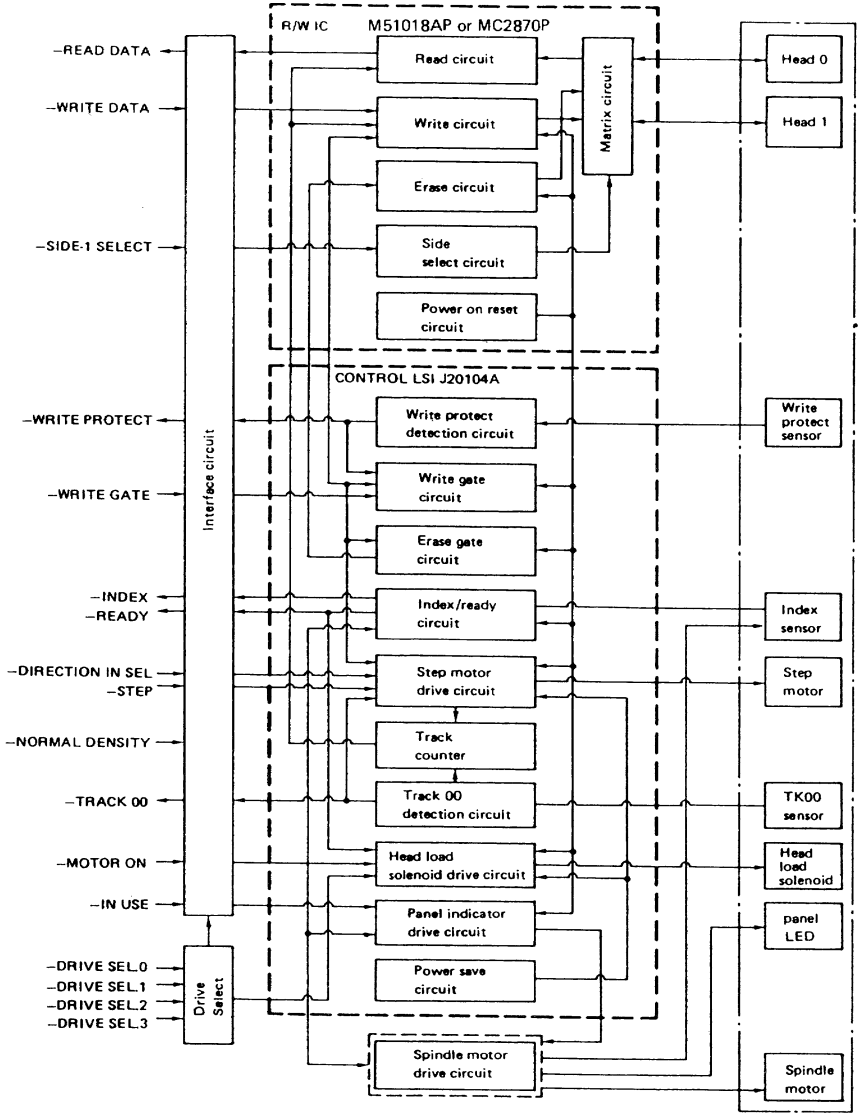


Figure 3-1 MF504A-3 Electronic Circuit

3-1 Interface and Drive Select Circuits

(1) Receive circuit

All the input terminals of the receiver that receives signals from the host controller are terminated at 150 ohms, pulling them up to +5 V. The host controller, therefore, must use driver elements with a drive capacity of 40 mA or more. Normally, an SN7438N or an equivalent open-collector drive is recommended. In connecting two or more disk drives (up to four) by a daisy-chain pattern, it is necessary to keep the cable end terminating resister and remove the terminating resistors of the other disk drives.

(2) Transmit circuit

The disk drive line driver is an SN7438N or equivalent open-collector gate. It is necessary for the host controller to use a terminating resistor of 150 ohms or more.

All input signals to the line driver are gated by drive select signals. Thus, if two or more disk drives are connected in the daisy-chain pattern, the signals of only one selected disk drive are transmitted to the host controller.

(3) Drive select circuit

The drive select circuit selects one of the disk drives (four maximum) connected with the same cables through four interface lines (DS0 through DS3).

The four select lines correspond to the jumper plugs on the printedcircuit boards, one of which should be inserted to select the desired line. Never insert plugs into the same-numbered jacks on two or more disk drives that are connected with the same cable; interference between the output signals from such disk drives will cause errors.

The drive select signals also light the panel indicator LED.

In the case of a system requiring no drive selection, insert the jumper plug for the drive select line into the MX to maintain a selected condition.

3.2 Power-On Reset and Power Save Circuits

(1) Power-on reset circuit

The power-on reset circuit, a level-detection type reset circuit, initializes the control LSI, and that's used for preventing operation errors of the write circuit in switching power on, off.

(2) Power save circuit

The power save circuit controls current flowing to the step motor and head load solenoid according to their operating condition to reduce heat generation by unnecessary power consumption and thus to reduce temperature rise of the disk drive.

The step motor and head load solenoid share the same timer (mono-stablemultivibrator), which has a range of 30 ms.

Timing chart of the power save circuit is shown in figure 3-2.

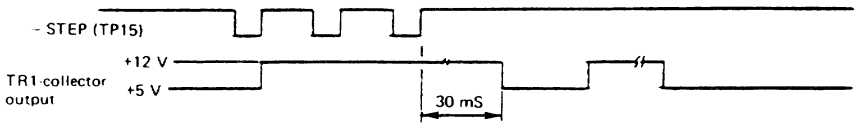


Figure 3-2 Power Save Circuit Timing Chart

3.3 Panel Indicator Circuit

The panel indicator is turned on by a drive select signal or by a drive select signal and in-use signal.
When no in-use signal is applied to the interface, the panel indicator is turned on by a drive select signal only.
If the jumper plug for the drive select circuit is inserted into the MX, the panel indicator is turned on by an in-use signal only.

Regarding jumper plug combination and indicator conditions, refer to the detailed description in the Standard Specifications MF504A-3.

3.4 Index Sensor and Ready Circuits

The index sensor circuit detects the index holes in the disk with a sensor, and converts its signals into logic signals.
The ready circuit checks the index pulse intervals with a timer, and becomes ready when the intervals are less than 300 ms and the next index pulse is generated.
When the door opens and the disk stops rotating and the motor-on signal turns off and the disk stops rotating the ready signal is reset.
Figure 3.3 shows a timing chart.

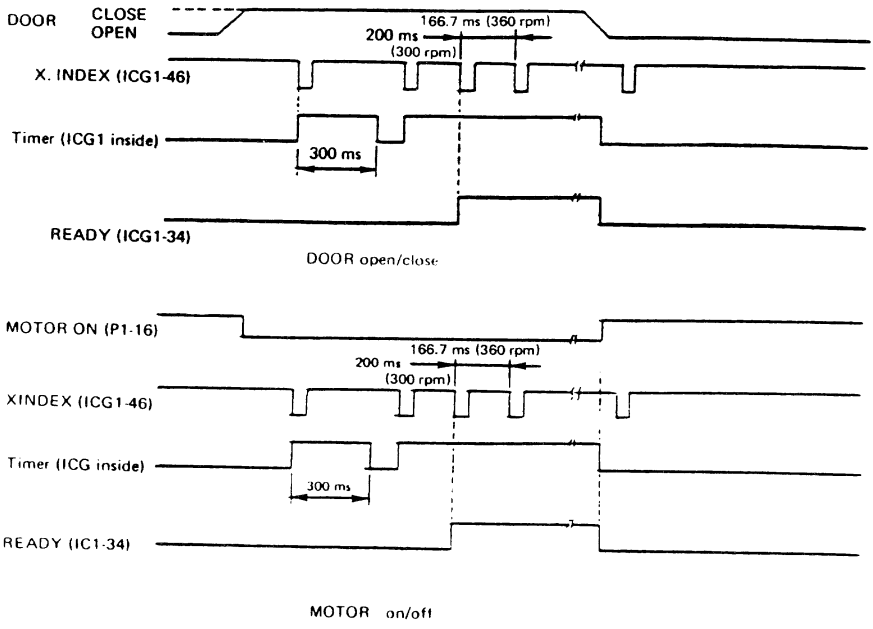


Figure 3-3 Index Sensor and Ready Circuit Timing Chart

3.5 Step Motor Drive Circuit

The step motor is a two-phase bipolar type and is driven to a step angle of 1.8° by feeding four mode currents, using two source/sink type drivers.
These four modes are generated by an up-down four-court counter that uses two flip-flops.
The step motor drive circuit switches the voltage supplied to the motor drive circuit to reduce power consumption during times other than seeking, when the motor is still.
In a seek operation, +12 V is supplied to the drive circuit, but if the next step pulse is not applied to the interface for 30 ms or more, +5 V is supplied.
Figure 3-4 shows a timing chart.
The step motor drive circuit blocks the step pulses with a write gate (except for the erase delay time) to prevent seeking during write operation. When the track 00 sensor output turns on, the circuit also blocks the step pulses to prevent further outward seek.

3.6 Track 00 Detection Circuit

The track 00 detection circuit detects the position of the light-shielding plate that projects from the head/carriage assembly, using a sensor. This output is ANDed with the step motor drive phase (TK00) to generate a track 00 signal. The circuit will not output a signal, therefore, unless the drive phase is at track 00 even if the sensor output is on.
For a timing chart, refer to figures 3-4.

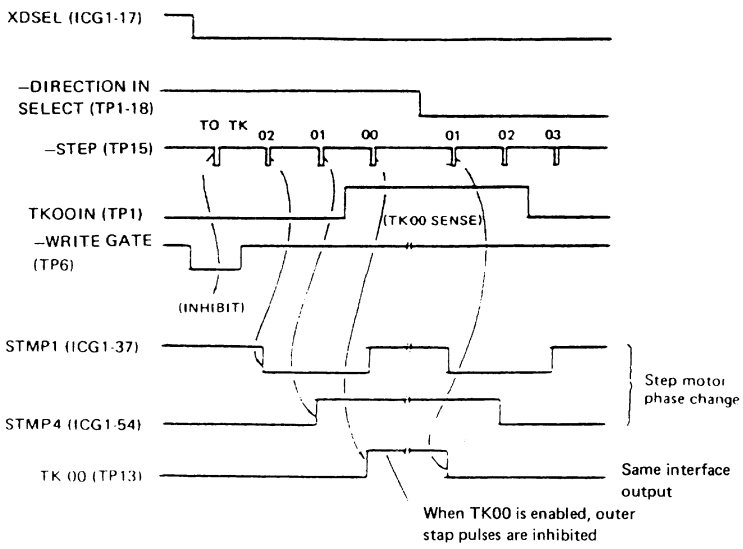


Figure 3-4 Step Motor Drive Circuit Timing Chart

3.7 Side Select Circuit

Side selection is made by switching the head center tap from about 0 V at off to about 11 V at on.
This operation alternately feeds a write current from center tap CT-0 (CT-1) to H0A (H1A) and H0B (H1B), and an erase current from center tap CT-0 (CT-1) to ER-0 (ER-1) during write operation. In read operation a bias currents is fed from CT-0 (CT-1) to HO'A (H1A) and H0B (H1B) to induce a voltage between H0A (H1B) and H0B (H1B).
The host system selects side 1 through the interface line if – SIDE ONE SELECT is low, or side 0 through the same interface line if it is high.
Figure 3-5 shows a block diagram of the side select circuit.

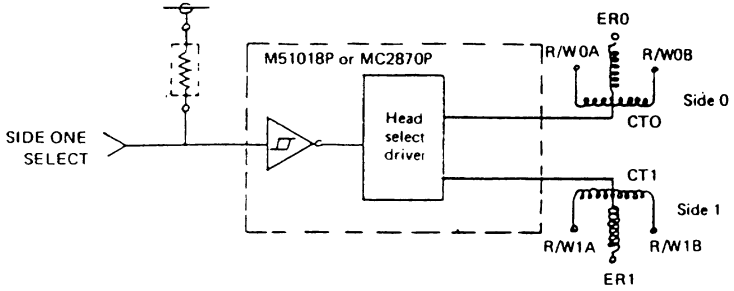


Figure 3-5 Side Select Circuit Block Diagram

3.8 Write/Erase Circuits

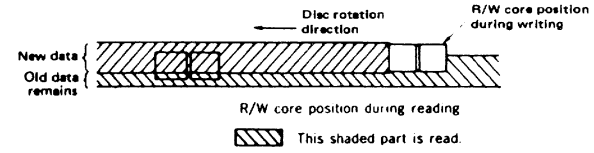
The write circuit is used for recording data on the disk. It starts writing when the write gate is opened for the selected head. If diskette write-protect status is detected, no write operation is performed.
The erase circuit erases the previous data written on both sides of the data by DC erasure. This function prevents old data from remaining on either side of newly written data due to a slight deviation of head position, and thus prevents old data crosstalk in reading the new data.
The write circuit consists of the following blocks:

- Write toggle flip-flop
- Write driver
- R/W matrix
- Write current source

When a write gate is input, the write toggle flip-flop, write driver and write current source are enabled to start a write operation. Write data is counted down to one half by the write toggle flip-flop, and a differential signal that changes synchronously with the write data is generated.
This differential signal switch the write driver.
The write driver is a switching circuit that feeds a current to the R/W head. This current is generated by the write current source and is sent to the write driver.
The R/W matrix feeds a current to the head selected by SIDE ONE SELECT as the write circuit gate is opened by a write gate.
Figure 3-6 shows the erase function and figure 3-7, a write circuit block diagram.

Current is alternately fed to the R/W head through two current routes, CT → R/WA and CT→ R/WB as shown in the figure, according to the differential signal to invert its magnetization.
Erase operation starts with point E befor write start point C and ends at point F after write end point D. The circumferential position deviation of the R/W core from the erase core is about 0.6 mm, and the erase core reaches a point that the R/W core gap has passed approx. 350μs at 360rpm (approx. 500μs at 300rpm) later (near TK 32). Therefore, the delay operation shown in figure 3-9 is required for the time from the opening of the write gate to the turning on of the erase driver and from the closing of the write gate to the turning off of the erase driver. It is for this purpose that the erase delay timer is provided to control the erase driver. Thus, for approx. 590μs at 360rpm (approx. 1000μs at 300rpm) after the closing of the write gate, the head must remain on the track and be kept selected.
The erase function erases data from the disk by always magnetizing it in one direction.
Figure 3-8 shows a conceptual diagram of write operation and figure 3-9, an erase delay operation timing chart.

(Without erase head)



(With erase head)

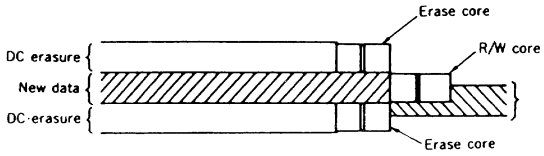


Figure 3-6 Erase Function

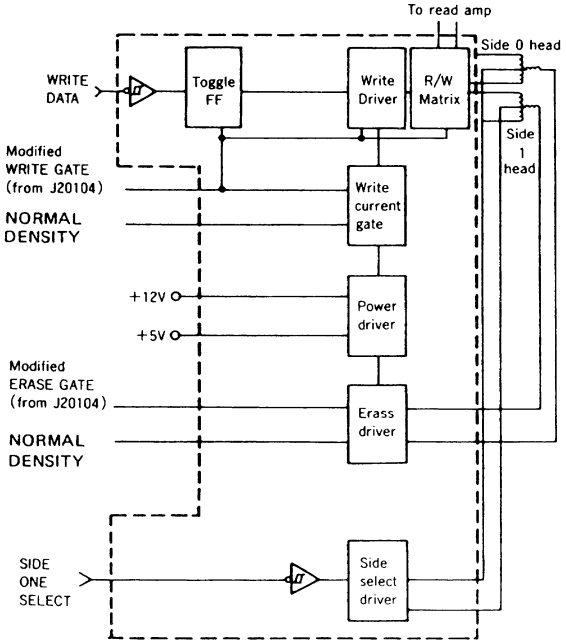


Figure 3-7 Write Circuit Block Diagram

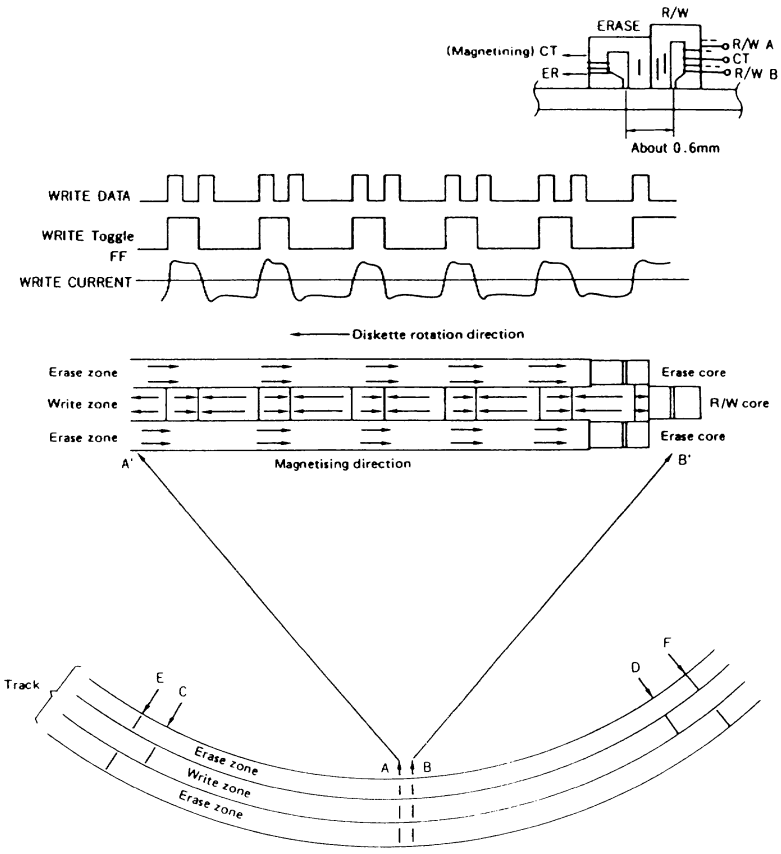


Figure 3-8 Write Operation Concept

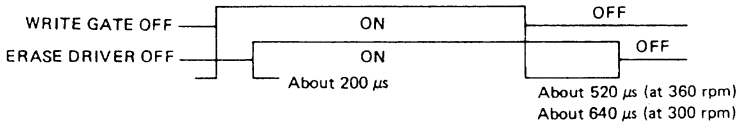


Figure 3-9 Erase Delay Operation Timing Chart

3.9 Write-Protect Circuit

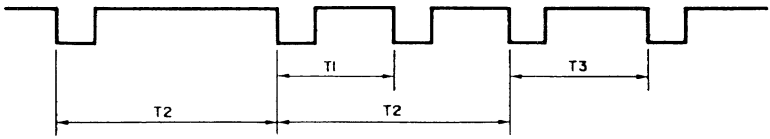
The write-protect circuit detects the notch (cutout in the jacket) of the diskette with a sensor to inhibit write operation even if a write gate signal is received from the interface, and outputs a write-protect signal to the interface. Figure 3-16 shows a circuit diagram of the write-protect circuit.

3.10 Read Circuit

The diskette is read when the write gate and erase driver are closed.
The R/W core is on a track. If a head has been selected, the core reads the inversions of magnetization of the previously written data to induce a voltage between the two ends of the R/W coil (between R/WA and R/WB). This voltage is input to the read preamplifier via the R/W matrix.
The read preamplifier provides a gain about 200 times the level of a few millivolts induced in the head, and amplifies the input into a differential signal high enough for signal processing.
The read signal from the read preamplifier is fed through a low-pass filter that cuts out excess high frequencies. The low pass filter is constructed so that it is automatically switched for high/normal density. It is thus, matched for the optimum frequency of each of the two.
Because the position of inverting magnetization is expressed by a read signal peak, the read signal is fed to a peak-detection circuit to generate a read data pulse.
The peak-detection circuit consists of three blocks.

- Differentiator
- Comparator
- Time domain filter

The differentiator is a differentiating circuit to detect the peak point, and the detected peak point is converted to a zero-crossing point. The differentiated signal is routed to the comparator, where it is converted from an analog signal to a digital signal. The point of change of this digital signal actually becomes a data pulse. FM or MFM means frequency modulation. The frequency of magnetization inversion intervals used are in figure 3-10.



	MFM			Highest frequency
	FM			
	T1	T2	T3	(at T1)
High density 360rpm	2.0 μs	4.0 μs	3.0 μs	250 kHz
Normal density 300rpm	4.0 μs	8.0 μs	6.0 μs	125 kHz
Normal density 360rpm	3.3 μs	6.7 μs	5.0 μs	150 kHz

Figure 3-10 DATA Timing

Adjacent magnetization inversion waveforms interfere with the magnetization inversion waveform converted from magnetism to an electronic signal, so their combined waveform is read. If magnetization inversion intervals lengthen, however, the mutual interference decreases, resulting in generating a shoulder. When a shoulder is generated, the differentiated waveform zero-crosses so that the wrong data pulse is detected. A time domain filter is provided for removing the wrong data pulse. The time domain filter is constructed so that it is automatically switched for high/normal density. It is thus, set for the optimum frequency for each of the two.

If the comparator output maintains the level prior to the single operation ① following the zero crossover point for a specific amount of time, the time domain filter generates that output as real read data ② .

The read data thus generated is sent to the host system. Figure 3-11 shows a read circuit block diagram and figure 3-12, a read timing chart.

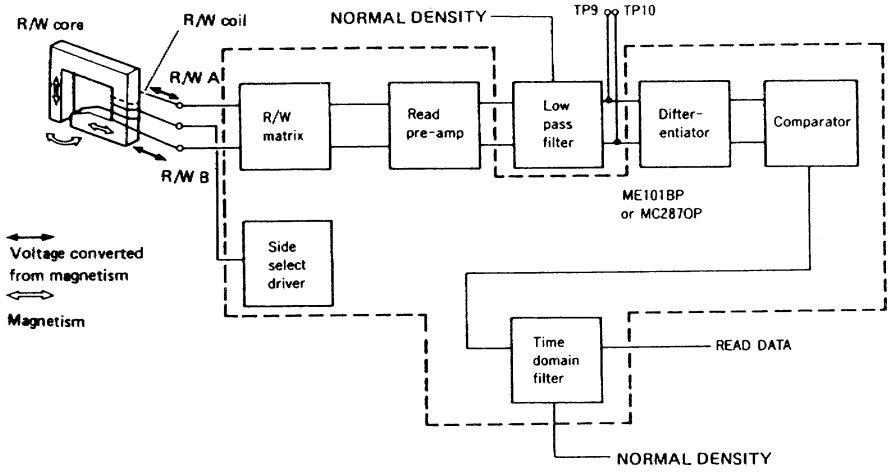


Figure 3-11 Read Circuit Block Diagram

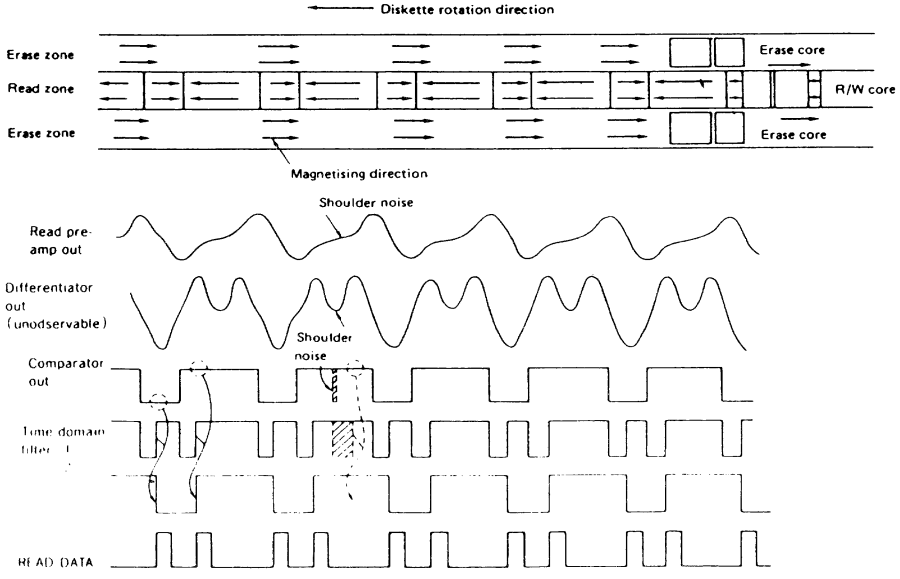


Figure 3-12 Read Timing Chart

3.11 Write current switch

The write is switched on this unit for the optimum recording current for both high and normal density disks.

(1) Write current switch
Write current for high density disks is set when the interface line is logical "1".
Write current for normal density disks is set when the interface line is logical "0".

3.12 Spindle Motor Drive Circuit

The spindle motor is a DC, direct, brushless motor for which a feedback servo circuit is employed to maintain the correct speed at all times. This circuit is installed on a separate printed-circuit board that is built integrally with the motor.

It is connected to the main control circuit with four signal lines: +12 V DC, 0 V, motor-on signal, and IN USE LED.

This feedback servo circuit employs Hall elements for position feedback and a frequency generator, or tachometer generator, for speed feedback to constitute a secondary system to stabilize motor rotation.

Spindle rotating position is detected by the Hall elements located symmetrically from the rotating spindle, and the information is fed to the predriver to alternately switch driver 1 and driver 2.

The speed signal output by the frequency generator for speed control is rectified and integrated into a speed voltage, which is compared with the reference speed voltage to feed back the level of current to be supplied to the coil. The rotational speed of the motor is switched by changing the reference speed value.

Figure 3-13 shows a spindle motor drive circuit block diagram and figure 3-14, a conceptual diagram of the spindle motor drive circuit waveforms.

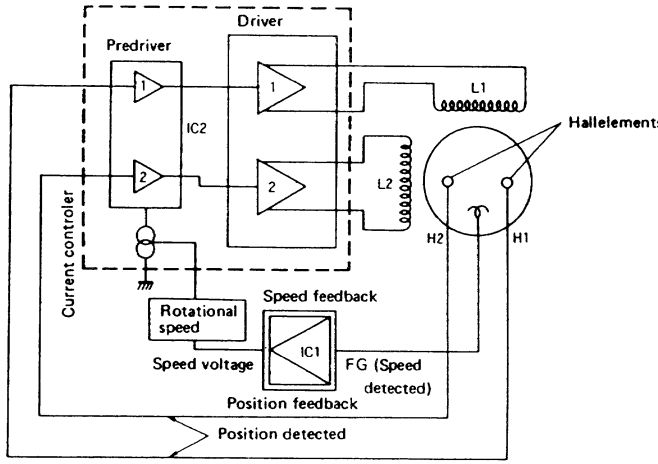


Fig. 3-13 Spindle motor drive circuit block diagram

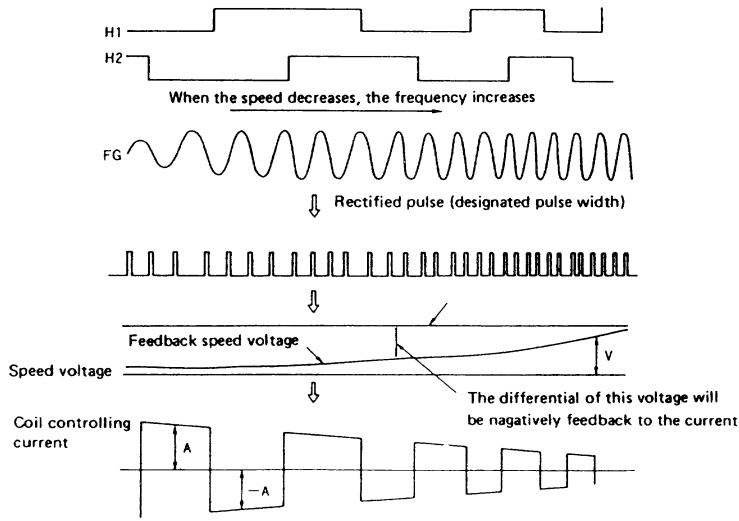


Fig. 3-14 Spindle motor drive current wavefrom configuration